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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/420,086	10/18/1999	WARREN M. FARNWORTH	98-0105.01	2322

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/420,086	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-39 and 47-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-39 and 47-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. Claim limitations as recited in claim 25, line 3, include: "chip scale surface".

However, it is not clear from Fig. 7B/specification, how the substrate surface of the BGA package (see Fig. 7B; specification pp. 14) is considered as being the chip scale surface.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 25-37, 29-33, 35, 36, 38, 39 and 47-53, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) in view of Liu et al. (US Pat. 5693568).

Regarding claims 25-27 and 29, Chou et al. disclose a semiconductor component/assembly/package (1000 in Fig. 10A/10B; Col. 16, lines 5-21) comprising:

- a substrate made of material such as a printed circuit board (PCB), plastic/epoxy laminate, ceramic, etc. (not numerically referenced in Fig. 10A/10B- Col. 1, line 53, Col. 10, line 29, Col. 16, line 46) having top and bottom surfaces
- the top surface/chip scale surface having dimensions such that it can be expressed by comparison with a chip unit/chip scale
- a conductive layer on the top surface comprising a metal alloy/conductive layer of a predetermined/selected thickness (see 512/1011a-1011d in Fig. 10A/10B; Col. 10, lines 30-53) having elements/land segments comprising a plurality of first portions (1011a and 1011d in Fig. 10A/10B) and a plurality of second portions (1011b, 1011c and 512 in Fig. 10A/10B), the metal alloy comprising a conventional material such as copper (Col. 10, line 38, Col. 17, line 32)
- a plurality of conductors on the first and second portions comprising conductive pads/sites (not numerically referenced- see bonding pads/sites on 1011a, 1011b, etc. connected by bonding wires in Fig. 10A), those on the first portions being separated and electrically isolated from one another by those on the second

portions of the conductive layer (see 1011a/1011d being spaced from 101 lb in Fig. 10A/10B)

- a plurality of recesses/grooves having equal width through/in the conductive layer (not numerically referenced- see recesses/grooves having the desired size, shape and width in Fig. 10A/10B between the conductive portions of the conductive layer), the grooves/recesses defining a size, a spacing and a shape (Col. 11, lines 20-24) of the conductors and the second portions of the conductive layer
- a semiconductor die (die 502 in Fig. 10A/10B) being mounted on the top surface of the substrate in an electrical communication with the conductors comprising conductive portions/conductive pads which are defined by respective grooves/recesses
- a plurality of electrically conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the conductors/conductive pads (1011a, 101 lb, etc. respectively in Fig. 10A), and
- a plurality of external contacts/balls (not numerically referenced in Fig. 10A- see 522a-522e in Fig. 5B; Col.16, lines 46-53) in a ball grid array (BGA) on the bottom surface of the substrate, the external contacts/balls being in electrical communication with the respective conductive vias and conductive portions of the conductive layer (Col. 16, lines 33-38)

(Fig. 10A/10B; Fig. 5A-5G; Col. 16, line 5- Col. 17, line 37).

Chou et al. further teach using a reduced pitch between the lands/pads and using shorter bonding wires to provide reduced impedance and improved manufacturing yield and reliability (Col. 16, line 55- Col. 17, line 37).

Chou et al. fail to teach:

a) the conductors and the second portions substantially covering the surface of the substrate and the plurality of first and second portions of the conductive layer being configured for electrical transmission and no electrical transmission respectively, and

b) each groove having a micron sized width.

a) Chou et al. further teach in another embodiment (Fig. 11A/11B), the conductive layer being extended to include a thermally and an electrically conductive die attach/paddle metal area (Col. 17, lines 16-50), the die attach/paddle metal area being selectively connected with one or more of the land segment/pad region of the first or second portions of the conductive layer to provide a significant increase in the area covering the surface of the substrate and to provide the enhanced thermal dissipation and heat transfer from the die (Col. 17, lines 50-65). Such land/pad connections further comprise one or more connections configured for grounded/no electrical transmission separated by those configured for electrical transmission (see Col. 16, line 5- Col. 17, line 50).

Furthermore, determination of parameters such as conductor dimensions including conductor area, thickness, width/spacing, shape/profile, etc., die pad area, pad/via dimensions, number of such conductors/pads/vias, etc. in chip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired electrical characteristics including impedance, signal-to-noise ratio, grounding, etc., operating speed, performance and reliability.

b) Liu et al. teach conventional semiconductor packages comprising conductor/interconnect pattern having feature size/width and spacing being 0.3-0.4 microns or greater) or having conductor width/spacing as low as 0.35 microns or less to improve operating speed and to reduce signal-to-noise ratio (Col. 1, lines 57-64; Col. 3, lines 50-67). Such dimensions/ground rules of the conductor can be achieved/facilitated by using conventional methods such as I-line/deep UV photolithography and plasma/reactive ion etching, laser machining, etc.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the elements a) and b) and the width of each groove/conductor being equal or about 5 microns as taught by the embodiment of Fig. 11A/11B in Chou et al. and Liu et al. so that the thermal dissipation, speed/performance and electrical performance/grounding can be improved and the desired impedance value can be achieved in Chou et al's component.

Regarding claim 29, selecting the thickness/width dimension of the conductors to form the grooves do not distinguish over Chou et al. and Liu et al., because only the final product/structure is relevant, not the process of forming the grooves such as "selecting the thickness/width to facilitate deep UV-photo processing/plasma etching or E-beam exposure/reactive ion-etching or sputtering" or "laser machining". Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claims 30, 31, 35, 38, 39, 52 and 53, Chou et al. and Liu et al. teach substantially the entire claimed structure as applied to claims 25-27 and 29 above.

Regarding claim 32, Chou et al. and Liu et al. teach substantially the entire claimed structure as applied to claims 25 and 30, wherein Chou et al. teach the plurality of conductive vias through the substrate (1034a, 1034b, etc. in Fig. 10A/10B) in electrical communication with the respective conductors (1011a, 1011b, etc. respectively in Fig. 10A) and the plurality of external contacts/contact balls (not numerically referenced in Fig. 10A- see 522 a-522e in Fig. 5B; Col.16, lines 46-53) on the bottom/second surface of the substrate.

Regarding claims 33 and 36, Chou et al. and Liu et al. teach substantially the entire claimed structure as applied to claims 25, 30 and 35, wherein Chou et al. teach the component comprising the assembly/package (1000 in Fig. 10A/10B; Col. 16, line 39).

Regarding claims 47-50, Chou et al. and Liu et al. teach substantially the entire claimed structure as applied to claims 25-27 and 29 above, wherein Chou et al. teach the each conductor having opposing edges (see vertical edges of 1011a-1011d in Fig. 10A) being defined by a pair of grooves/recesses (see the pair of grooves/recesses on both sides of 1011a-1011d in Fig. 10A) and each conductor having the portions of the conductive layer on either side being separated from the opposing edges by the pair of grooves/recesses.

Regarding claim 51, Chou et al. and Liu et al. teach substantially the entire claimed structure as applied to claim 47 above, wherein Chou et al. teach the conductive layer (512/1011a-1011d in Fig. 10A/10B) having an opening in a central portion for attaching/bonding the die to the substrate (see Fig. 10A).

5. Claim 28, insofar as being in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) and Liu et al. (US Pat. 5693568) as applied to claim 25 above, and further in view of Hembree (see prior art-IDS, US Pat. 5783461).

Regarding claim 28, Chou et al. and Liu et al. teach substantially the entire claimed structure as applied to claim 25 above, except at least one semiconductor die comprising a plurality of bumps bonded to the pads.

Hembree teaches a package wherein a semiconductor die is connected to a substrate using conventional wire bonding or flip chip bonding/mounting with a plurality of pads/bumps to the respective plurality of bond pads on the conductors/substrate (see 56/60 in Fig. 4; Col. 6, line 21).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one semiconductor die comprising a plurality of bumps bonded to the pads defined by the grooves as taught by Hembree so that the

interconnect density can be improved and the processing can be simplified in Liu et al. and Chou et al's component.

6. Claims 34 and 37, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chou et al. (US Pat. 5691568) and Liu et al. (US Pat. 5693568) as applied to claims 30 and 35 above, and further in view of Pedder (US Pat. 5717245).

Regarding claims 34 and 37, Chou et al. and Liu et al. teach substantially the entire claimed structure as applied to claim 30, except an encapsulant at least partially covering the die and a portion of the surface.

Pedder teaches using a sealant/encapsulant to encapsulate the BGA package/module (Col. 1, line 55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the encapsulant covering the die and a portion of the surface as taught by Pedder so that the surface protection for the electrical connections can be improved and the damage from contamination and moisture can be reduced in Liu et al. and Chou et al's component.

Response to Arguments

7. Applicant's arguments with respect to claims 25-39 and 47-53 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

03-22-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800